IN THE CLAIMS

Please cancel claims 1-39.

Please add new claims 62-92.

62. (New) A method comprising:

a) driving a first current through a line and a termination resistance so that a logical value on said line changes from a first logical value to a second logical value, said first current sustained for a width of a first bit that is propagated on said line; and,

b) holding said second logical value on said line by driving a second current through said line and said termination resistance, said second current less than said first current, said second current sustained for a width of a second bit that is propagated on said line.

63. (New) The method of claim 62 wherein said first and second currents flow in a direction from said line into said termination resistance.

64. (New) The method of claim 63 wherein said second logical value is a logical high.

65. (New) The method of claim 63 wherein said first current produces a first voltage on said line that is larger than a second voltage produced on said line by said second current.

66. (New) The method of claim 62 wherein said first and second currents flow in a direction from said termination resistance into said line.

67. (New) The method of claim 66 wherein said second logical value is a logical low.

68. (New) The method of claim 66 wherein said first current produces a first voltage on said line that is smaller than a second voltage produced on said line by said second current.

69. (New) The method of claim 62 wherein said first bit width is coextensive with a clock cycle.

70. (New) The method of claim 62 wherein said driving a first current further comprises applying a first multiplexer select line state to a multiplexer so that a first word is provided at an output of said multiplexer, said first word enabling a first number of sub-drivers, and said driving a second current further comprises applying a second multiplexer select line state to said multiplexer so that a second word is provided at said output of said multiplexer, said second word

enabling a second number of said sub-drivers, said first number greater than said second number.

71. (New) An apparatus, comprising:

a driver that drives a line that is terminated with a termination resistance, said termination resistance coupled to a termination voltage, said driver designed to drive said line to a first voltage if a logical value on said line needs to be changed from a first logic level to a second logic level, said driver designed to drive said line to a second voltage if said second logic level on said line does not need to be changed, the squared difference between said first voltage and said termination voltage being greater than the squared difference between said second voltage and said termination voltage, said first and second voltages each capable of being interpreted as said second logic level.

72. (New) The apparatus of claim 71 wherein said first voltage is reached during a first bit width and said second voltage is reached during a second, following bit width.

73. (New) The apparatus of claim 71 wherein said driver further comprises a plurality of sub-drivers, each of said sub-drivers designed to drive said line, a first number of said sub-drivers designed to drive said line to said first voltage, a

second number of said sub-drivers designed to drive said line to said second voltage, said first number larger than said second number.

74. (New) The apparatus of claim 73 wherein said first number corresponds to all of said sub-drivers.

75. (New) The apparatus of claim 73 further comprising a multiplexer that alternatively issues a first word and a second word, said first word to enable said first number of said sub-drivers, said second word to enable said second number of said sub-drivers.

76. (New) The apparatus of claim 71 wherein said line is an address line that addresses a memory device.

77. (New) The apparatus of claim 76 wherein said second voltage appears on said line during the later cycles of a burst read from said memory.

78. (New) The apparatus of claim 77 wherein said memory is a DDR-SDRAM memory device.

79. (New) A method, comprising:

a) driving a line to a first voltage if said line's logic level needs to be changed from a first logic level to a second logic level, said line terminated

with a termination resistance, said termination resistance coupled to a termination voltage; and,

b) driving said line to a second voltage if said line's logic level does not need to be changed back to said first logic level after having been said changed from said first logic level to said second logic level, said first and second voltages capable of being interpreted as said second logic level, the squared difference of said first voltage and said termination voltage being greater than the squared difference of said second voltage and said termination voltage.

80. (New) The method of claim 79 wherein said first voltage is reached during a first bit width and said second voltage is reached during a second, following bit width.

81. (New) The method of claim 79 wherein said driving said line to said first voltage further comprises enabling a first number of sub-drivers, said driving said line to said second voltage further comprises enabling a second number of said sub-drivers, said first number larger than said second number.

82. (New) The method of claim 79 further comprising issuing a first word from a multiplexer in order to said enable said first number of sub-drivers and issuing a second word from a multiplexer in order to said enable said second number of said sub-drivers.

83. (New) The method of claim 79 wherein said line is an address line that addresses a memory device.

84. (New) The method of claim 83 wherein said second voltage appears on said line during the later cycles of a burst read from said memory.

85. (New) The method of claim 84 wherein said memory is a DDR-SDRAM memory device.

86. (New) An apparatus, comprising:

a) means for driving a line to a first voltage if said line's logic level needs to be changed from a first logic level to a second logic level, said line terminated with a termination resistance, said termination resistance coupled to a termination voltage; and,

b) means for driving said line to a second voltage if said line's logic level does not need to be changed back to said first logic level after having been said changed from said first logic level to said second logic level, said first and second voltages capable of being interpreted as said first logic level, the squared difference of said first voltage and said termination voltage being greater than the squared difference of said second voltage and said termination voltage.

87. (New) The apparatus of claim 86 wherein said first voltage is reached during a first bit width and said second voltage is reached during a second, following bit width.

88. (New) The apparatus of claim 86 further comprising means for driving said line to said first voltage with a first number of sub-drivers, and comprising means for said driving said line to said second voltage with a second number of sub-drivers, said first number larger than said second number.

89. (New) The apparatus of claim 88 further comprising means for issuing a first word in order to said enable said first number of sub-drivers and issuing a second word in order to said enable said second number of sub-drivers.

90. (New) The apparatus of claim 86 wherein said line is an address line that addresses a memory device.

91. (New) The apparatus of claim 90 wherein said second voltage appears on said line during the later cycles of a burst read from said memory.

92. (New) The apparatus of claim 90 wherein said memory is a DDR-SDRAM memory device.